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(71) Applicant : **TEXAS INSTRUMENTS INCORPORATED**
13500 North Central Expressway
Dallas Texas 75265 (US)
(84) **DE FR IT NL**

(71) Applicant : **TEXAS INSTRUMENTS LIMITED**
Manton Lane
Bedford MK41 7PA (GB)
(84) **GB**

(72) Inventor : **Pathak, Vijay, c/o Texas Instruments Ltd.**
Manton Lane
Bedford MK41 7PA (GB)

(74) Representative : **Abbott, David John et al**
Abel & Imray
Northumberland House
303-306 High Holborn
London, WC1V 7LH (GB)

(54) Improvements in or relating to multi-slot input/outputs.

(57) An I/O structure for a device comprising at least one input/output pad ; a power supply pad and input/output buffer, wherein the I/O buffer extends in a peripheral direction to a great extent that it extends inwardly, with respect to the device. One of the advantages of this is that there is a saving in the amount of silicon used for the I/O structure. In addition, the I/O structure of the present invention has improved performance for high speed and high differential inputs and outputs.

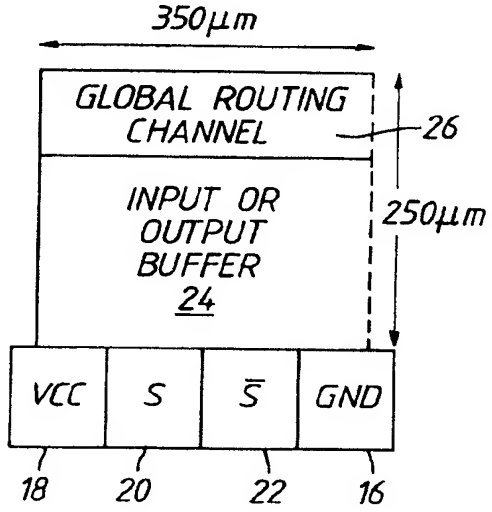

Fig.5b

EP 0 660 410 A2

The proposed invention relates to Input/Output (I/O) structures enabling significant savings in silicon chip area. The proposed structures are particularly suitable for high speed differential input/output interfaces such as those used in ATM/SDH switching elements.

Conventional I/O structures in differential and single ended configuration are shown in Figure 1(a) and 1(b) respectively. These consist of an I/O buffer cell which contains the input or output or input/output (in the bi-directional case) circuits to provide the desired functionality. In addition, power/ground busses are routed over the I/O buffer cells to feed power to the I/Os and to the core. Sometimes global signals such as a clock and a bias reference voltage are also routed over the I/O cells.

The pad cell is made up of a bonding pad and can also include an ESD rotection circuit.

The height (H) and the width (W) of the I/O typically depends upon one or more factors. One such factor is the number of interface pins required for the chip. The larger the pin count is, the narrrower the I/O has to be to maximise the pin count.

Another significant factor is the minimum width of the I/O. This is determined by bonding and assembly limitations.

The width of the power busses is also a factor which effects the overall height and width of the I/O. The width of the power busses is governed by the core and I/O current requirements and the metal electromigration capability of the process technology.

In addition, both the circuit requirements for I/O functionality and ESD functionality and the global signal routing also contribute to the overall width and/or the height of the I/O.

In general, the number of interface pins and the minimum width of the I/O have greater influence on the I/O width, whilst the other factors have greater influence on the height.

In addition to the I/O cells, the VCC and GND pads shown in Figure 2 and 3 respectively which are needed to feed the current in and out of the chip normally use one I/O slot (i.e. one width of the I/O). Thus in a high performance design where a large number of VCC and GND pins are required to the switching noise and power supply voltage drops, a large proportion of chip area is sacrificed for geometrical compatibility of VCC/GND pads with the input/output pads. An example of part of a conventional layout involving large number of differential I/Os and power/ground-pads is shown in Figure 4. The shaded area represents the silicon area sacrificed for geometrical compatibility described above.

One object of the present invention is to provide an I/O structure which overcomes at least some of the disadvantages of present structures.

According to one aspect of the present invention, there is provided an I/O structure for a device comprising at least one input/output pad; a power supply pad and input/output buffer, wherein the I/O buffer extends in a peripheral direction to a great extent that it extends inwardly, with respect to the device.

Preferably the at least one input/output pad comprises a differential pair of signal pads, which are respectively input/output and complementary input/output; and the power supply comprises a ground pad and a supply voltage pad.

Advantageously, the width of the input/output buffer is juxaposed along the width of the at least one input/output pad and at least some of the width of the power supply pad.

One of the advantages of this is that there is a saving in the amount of silicon used for the I/O structure.

In addition, the I/O structure of the present invention has improved performance for high speed and high differential inputs and outputs.

Reference will now be made, by way of example to the accompanying drawings, in which:

Figure 1a is a schematic representation of a known single ended I/O;

Figure 1b is a schematic representation of a known differential I/O;

Figure 2 is a schematic representation of a known Vcc cell;

Figure 3 is a schematic representation of a known Ground cell;

Figure 4 is a conventional layout involving a large number of differential I/Os, Vcc and Ground cells;

Figure 5a is a footprint of a conventional differential I/O; and

Figure 5b is a multislot I/O according to one aspect of the present invention.

Referring to Figure 4 part of a known I/O structure 10 is shown. The structure 10 comprises a core 12 and a plurality of pads 14 around the edge of the layout. The pads include ground pads 16, Vcc pads 18 and signal pads 20, 22. Associated with each pair of signal pads is an input/output buffer 24. The buffer is associated only with the signal pads and is juxaposed thereto along the width of the pads. A global signal routing channel (26) is also included to carry Vcc busses, Ground busses, bias lines (if required), etc. Since the buffer is not required for the Vcc and GND pads there is a large area of silicon 28 (shown shaded in Figure 4) which is wasted. This area 28 is sacrificed for geometrical compatibility.

The proposed invention makes use of this shaded area by altering the aspect ratio (ratio of width to height) of the I/O buffers whilst maintaining the power feed capabilities of the structure. Increasing the differential I/O buffer width from two slot equivalent to approximately 4 slots, will halve the I/O buffer height which in turn reduces the I/O height. For example, as shown in Figure 5, by increasing the differential I/O width from 200um to approximately 350um, the I/O

height can be reduced from 450um to 250um. As can be seen in Figure 5b, the overall height of the I/O structure is reduced but the area of the buffer is maintained. The buffer 24 extends along the width of the Vcc (18), Ground (16) and signal pads (20, 22). By providing the buffer in this way, the silicon area wasted by provision of the Vcc and ground pads is minimised. In addition, since a pair of power/ground pins feeds only one or a few differential pairs, the width of VCC/GND busses need not be as wide as used in the conventional designs which in turn helps reduce the I/O height.

The proposed I/O layout scheme is particularly useful for high speed designs requiring high differential inputs and outputs. The concept can also be extended to other applications where high speed interface is limited to a few sides of the chip. Even for single ended I/Os operating at speeds in excess of 100 Mhz, a large number of power/ground pins are required to minimise the simultaneous switching noise. The proposed invention can be utilised to widen the I/O buffer layout.

Using this approach, silicon saving up to 15% has been made in Siemens KNE design. The design is implemented as a test chip (X1444) in 0.6um EPIC-3B BiCMOS technology.

The I/O structure can be used on any device which requires an I/O structure.

Claims

1. An I/O structure for a device comprising:
   at least one input/output pad;
   a power supply pad and input/output buffer, wherein the I/O buffer extends in a peripheral direction to a great extent that it extends inwardly, with respect to the device.

2. A structure according to claim 1 wherein the at least one input/output pad comprises a differential pair of signal pads.

3. A structure according to claim 2, wherein the signal pads are respectively input/output and complementary input/output.

4. A structure according to any preceding claim, wherein the power supply comprises a ground pad and a supply voltage pad.

5. A structure according to any preceding claim, wherein the width of the input/output buffer is juscaposed along the width of the at least one input/output pad and at least some of the width of the power supply pad.

6. A structure according to any preceding claim, further including a global signal routing channel.

7. A device including an I/O structure according to any preceding claim.

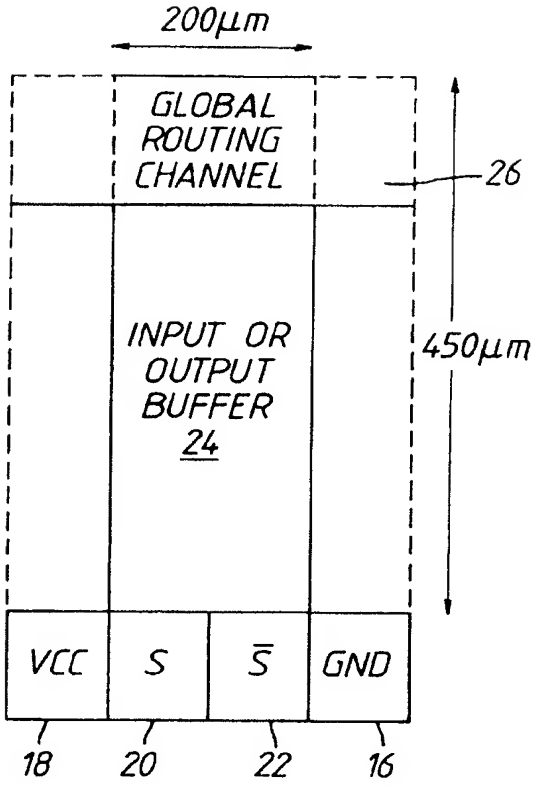
200µm
GLOBAL ROUTING CHANNEL
26
INPUT OR OUTPUT BUFFER 24
450µm
VCC
S
$\bar{S}$
GND
18
20
22
16

Fig.5a

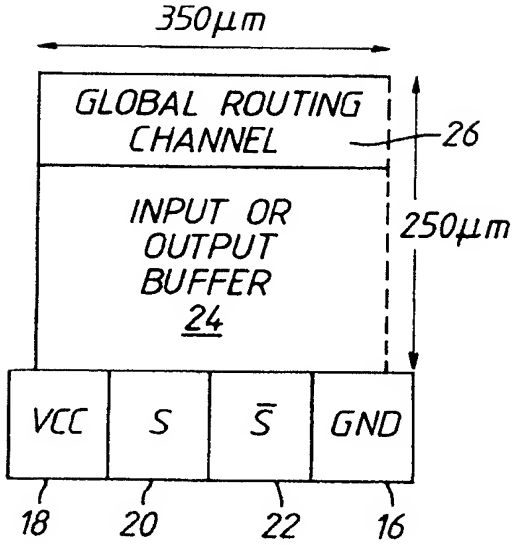
350µm
GLOBAL ROUTING CHANNEL
26
INPUT OR OUTPUT BUFFER 24
250µm
VCC
S
$\bar{S}$
GND
18
20
22
16

Fig.5b

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(71) Applicant : **TEXAS INSTRUMENTS INCORPORATED**
13500 North Central Expressway
Dallas Texas 75265 (US)
(84) **DE FR IT NL**

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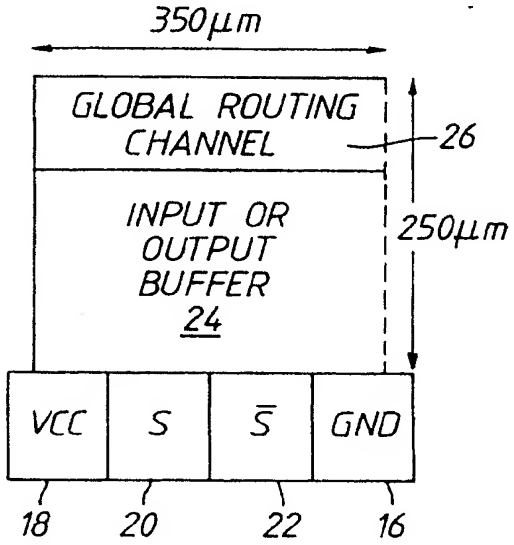

Fig.5b

EP 0 660 410 A3

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EUROPEAN SEARCH REPORT

Application Number EP 94308276.8

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 6)
X	PATENT ABSTRACTS OF JAPAN, unexamined applications, E field, vol. 12, no. 24, January 23, 1988, THE PATENT OFFICE JAPANESE GOVERNMENT page 43 E 576; & JP-A-62 179 744 (NEC)	1,7	H 01 L 23/58
Y	--	2-6	
Y	EP - A - 0 349 294 (HITACHI) * Abstract; fig. 1-6; column 4, line 5 - column 9, line 18 *	2-6	
A	--		
	US - A - 4 809 029 (MATSUMURA et al.) * Fig. 1,2,7; corresponding text *	1-7	
	----		TECHNICAL FIELDS SEARCHED (Int. Cl. 6)
			H 01 L G 11 C 11/00 G 06 F 13/00 H 03 K 17/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	30-05-1995	KUTZELNIGG

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

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E : earlier patent document, but published on, or after the filing date
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